Amendments to the Claims

1. (*Cancelled*)

2. (*Cancelled*)

3. (*Currently Amended*) ~~The converter of claim 2,~~ An integrated buck converter, comprising:

a controller; and

a plurality of circuits each operably connected to the controller, the plurality of circuits generate a plurality of current signals respectively and an output voltage signal;

wherein the controller and the plurality of circuits are integrated;

wherein the controller generates a plurality of drive signals to control the plurality of circuits respectively, the plurality of drive signals each having an associated phase;

wherein the output voltage signal is fed back to the controller;

wherein the controller comprises a duty cycle control circuit that compares the fed-back output voltage signal with a pre-selected reference voltage and adjusts a duty cycle value of the drive signals based on the comparison to maintain the output voltage signal at a desired level.

4. (*Original*) The converter of claim 3, wherein the plurality of drive signals have their associated phases overlapped one another if the duty cycle value multiplied by the number of the plurality circuits that are active is greater than one.

5. (*Currently Amended*) The converter of ~~claim 2,~~ claim 3,

wherein a sum of the plurality of current signals is fed back to the controller;

wherein the controller comprises a duty cycle control circuit that compares the sum of the fed-back current signals with a previous value of the sum and adjusts a duty cycle value of the drive signals based on the comparison.

6. (*Currently Amended*) The converter of ~~claim 2,~~ claim 3,

wherein the plurality of current signals are fed back to the controller;

wherein the controller comprises a duty cycle control circuit that calculates an average value of the fed-back current signals, compares the average value with each of the fed-back current signals and adjusts a duty cycle value for a corresponding drive signal based on the comparison.

7. (*Original*) The converter of claim 3, wherein the controller further includes:

a system clock circuit that generates system clock signals, and

a timing circuit, responsive to the duty cycle control circuit and the system clock circuit, that generates the drive signals in accordance with the duty cycle value provided by the duty control circuit.

8. (*Original*) The converter of claim 5, wherein the controller disables a selected number of the plurality of circuits when the sum of the plurality of current signals is below a predetermined value.

9. (*Original*) The converter of claim 8, wherein the controller disables the selected number of the plurality of circuits in proportion to a power level of the plurality of circuits.

10. (*Cancelled*)

11. (*Original*) ~~The converter of claim 10,~~ An integrated buck converter, comprising:

a controller; and

a plurality of circuits each operably connected to the controller;

wherein the controller and the plurality of circuits are integrated;

wherein the controller generates a plurality of drive signals to control the plurality of circuits respectively to generate a plurality of current signals and an output voltage signal, the plurality of drive signals each having an associated phase;

wherein the output voltage signal and a sum of the plurality of current signals are fed back to the controller;

wherein the controller comprises a duty cycle control circuit that compares the fed-back output voltage signal with a pre-selected reference voltage;

wherein the controller compares the sum of the fed-back current signals with a previous value of the sum;

wherein the controller adjusts a duty cycle value of the drive signals based on the voltage and current comparisons to maintain the output voltage signal at a desired level.

12. (*Original*) The converter of claim 11, wherein the controller further includes:

a system clock circuit that generates system clock signals, and

a timing circuit, responsive to the duty cycle control circuit and the system clock circuit, that generates the drive signals in accordance with the duty cycle value provided by the duty control circuit.

13. (*Original*) The converter of claim 11, wherein the controller disables a selected number of the plurality of circuits when the sum of the plurality of current signals is below a predetermined value.

14. (*Original*) The converter of claim 13, wherein the controller disables a selected number of the plurality of circuits in proportion to a power level of the plurality of circuits.

15. (*Original*) The converter of claim 11, wherein the plurality of drive signals have their associated phases overlapped one another if the duty cycle value multiplied by the number of the plurality circuits that are active is greater than one.

16. (*Original*) The converter of ~~claim 10,~~ claim 11,

wherein the plurality of current signals are fed back to the controller;

wherein the duty cycle control circuit calculates an average value of the fed-back current signals, compares the average value with each of the fed-back current signals and adjusts a duty cycle value for a corresponding drive signal based on the comparison.

17. (*Original*) The converter of claim 16, wherein the controller further includes:

a system clock circuit that generates system clock signals, and

a timing circuit, responsive to the duty cycle control circuit and the system clock circuit, that generates the drive signals in accordance with the duty cycle value provided by the duty control circuit.

18. (*Original*) The converter of claim 16, wherein the controller disables a selected number of the plurality of circuits when the sum of the plurality of current signals is below a predetermined value.

19. (*Original*) The converter of claim 18, wherein the controller disables a selected number of the plurality of circuits in proportion to a power level of the plurality of circuits.

20. (*Original*) The converter of claim 16, wherein the plurality of drive signals have their associated phases overlapped one another if the duty cycle value multiplied by the number of the plurality circuits that are active is greater than one.